IN THE CLAIMS:

Please note that all claims currently pending and under consideration in the referenced application are shown below, in clean form, for clarity.

1. (Three Times Amended) A semiconductor device assembly, comprising:

a semiconductor die having an active surface having a plurality of bond pads thereon and an opposing second surface;

at least one projection connected to at least one bond pad of said plurality of bond pads on the active surface of said semiconductor die directly connected to a substrate, said at least one projection including one of at least one solder ball and at least one solder bump; and

a generally centrally positioned paddle of a lead frame of a plurality of lead frames having side rails and cross members connected to said paddle, said second surface of said semiconductor die being secured to said paddle;

and said generally centrally positioned paddle being attached to the side rail by at least a plurality of paddle support bars and being attached to said cross members by said support bars.

2. The semiconductor device assembly of claim 1, wherein said at least one projection includes a plurality of projections comprising a ball grid array (BGA) of solder balls.

3. The semiconductor device assembly of claim 1, wherein said at least one projection comprises at least one ball deposited by a wire bonding machine.

4. The semiconductor device assembly of claim 1, wherein said at least one projection comprises at least one stud bump deposited by a wire bonding machine.

5. (Amended) The semiconductor device assembly of claim 1, further comprising: an electrically non-conductive adhesive layer securing said second surface to said generally centrally positioned paddle.

6. The semiconductor device assembly of claim 5, wherein said adhesive layer comprises one of epoxy and polyimide.

7. (Amended) The semiconductor device assembly of claim 1, further comprising: an electrically conductive adhesive layer securing said second surface of said semiconductor die to said generally centrally positioned paddle.

8. The semiconductor device assembly of claim 7, wherein said electrically conductive adhesive layer comprises a eutectic material.

9. The semiconductor device assembly of claim 7, wherein said electrically conductive adhesive layer comprises a gold-silicon eutectic material.

10. The semiconductor device assembly of claim 7, wherein said electrically conductive adhesive layer comprises a metal-filled polymer, said metal filling comprising a heat conductive material.

11. The semiconductor device assembly of claim 7, wherein said electrically conductive adhesive layer comprises conductive polyimide.

12. The semiconductor device assembly of claim 1, further comprising: said substrate having circuit connections, said plurality of bond pads bonded to said circuit connections.

13. The semiconductor device of claim 12, further comprising:
sealant packaging material enclosing a portion of said semiconductor die and covering a portion of said substrate.

14. (Three Times Amended) A semiconductor device assembly, comprising:
a semiconductor die having an active surface having at least one bond pad thereon and an opposing second surface;
at least one projection secured to said at least one bond pad on said active surface of said semiconductor die directly connected to a substrate, said at least one projection including one of at least one solder ball and at least one solder bump; and
a metal paddle from a lead frame, said second surface of said semiconductor die being attached to said paddle; and
said metal paddle is attached to at least one side rail by at least a plurality of paddle support bars and being attached to a plurality of cross members by said support bars.

15. The semiconductor device assembly of claim 14, wherein said at least one projection comprises a ball grid array (BGA) of solder balls.

16. The semiconductor device assembly of claim 14, wherein said at least one projection comprises at least one ball deposited by a wire bonding machine.

17. The semiconductor device assembly of claim 14, wherein said at least one projection comprises at least one stud bump deposited by a wire bonding machine.

18. The semiconductor device assembly of claim 14, further comprising:
an electrically non-conductive adhesive layer attaching said second surface to said paddle.

19. The semiconductor device assembly of claim 18, wherein said adhesive layer comprises one of epoxy and polyimide.

20. (Amended) The semiconductor device assembly of claim 14, further comprising: an electrically conductive adhesive layer attaching said second surface to said metal paddle.

21. The semiconductor device assembly of claim 20, wherein said electrically conductive adhesive layer comprises a eutectic material.

22. The semiconductor device of claim 20, wherein said electrically conductive adhesive layer comprises a gold-silicon eutectic material.

23. The semiconductor device assembly of claim 21, wherein said electrically conductive adhesive layer comprises a metal-filled polymer, said metal filling comprising a heat conductor.

24. The semiconductor device assembly of claim 21, wherein said electrically conductive layer comprises conductive polyimide.

25. The semiconductor device assembly of claim 14, further comprising:
a substrate having a plurality of circuit connections, said at least one bond pad connected to at least one circuit connection of said plurality of circuit connections.

26. The semiconductor device assembly of claim 25, further comprising:
sealant packaging covering a portion of said semiconductor die and a portion of said substrate.

27. (Three Times Amended) A semiconductor device assembly, comprising:

a semiconductor die having an active surface having a plurality of bond pads thereon and an opposing second surface;

a plurality of projections connected to said plurality of bond pads directly connected to a host circuit board, said plurality of projections including one of a plurality of solder balls and a plurality of solder bumps; and

a metallic paddle secured to said second surface of said semiconductor die, said metallic paddle being attached to at least one side rail by at least a plurality of paddle support bars and being attached to a plurality of cross members by said support bars.

28. The semiconductor device assembly of claim 27, wherein said plurality of projections comprises a ball grid array (BGA) of solder balls.

29. The semiconductor device assembly of claim 27, wherein said plurality of projections comprises balls deposited by a wire bonding machine.

30. The semiconductor device assembly of claim 27, wherein said plurality of projections comprises a plurality of stud bumps deposited by a wire bonding machine.

31. (Amended) The semiconductor device assembly of claim 27, further comprising:

an electrically non-conductive adhesive layer connecting said second surface to said metallic paddle.

32. The semiconductor device assembly of claim 31, wherein said adhesive layer comprises one of epoxy and polyimide.

33. (Amended) The semiconductor device assembly of claim 27, further comprising: an electrically conductive adhesive layer connecting said second surface to said metallic paddle.

34. The semiconductor device assembly of claim 33, wherein said electrically conductive adhesive layer comprises a eutectic material.

35. The semiconductor device assembly of claim 33, wherein said electrically conductive adhesive layer comprises a gold-silicon eutectic material.

36. The semiconductor device assembly of claim 33, wherein said electrically conductive adhesive layer comprises a metal-filled polymer, said metal filling comprising a heat conductive material.

37. The semiconductor device assembly of claim 33, wherein said electrically conductive adhesive layer comprises conductive polyimide.

38. The semiconductor device of claim 27, further comprising:
a substrate having a plurality of circuit connections, said plurality of bond pads connected to said plurality of circuit connections.

39. The semiconductor device assembly of claim 38, further comprising:
sealant packaging covering a portion of said semiconductor die and a portion of said substrate.